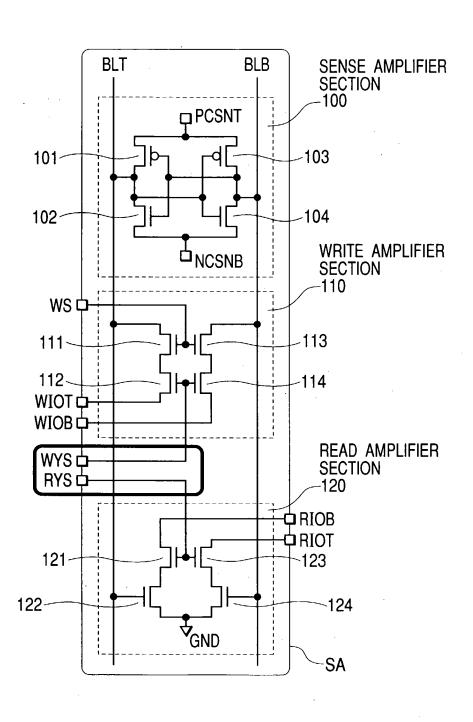


FIG. 1



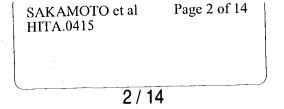
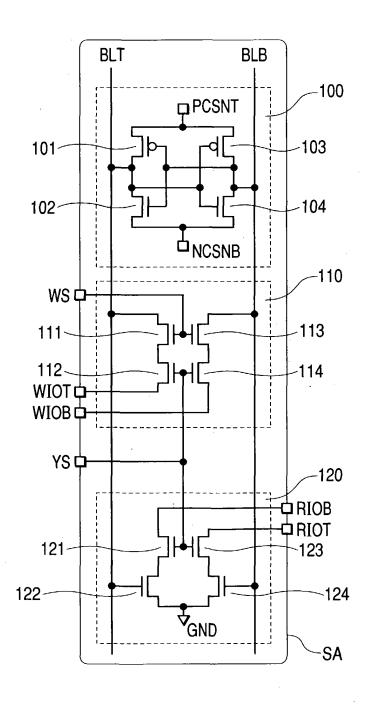
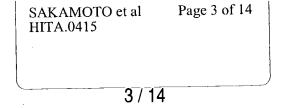
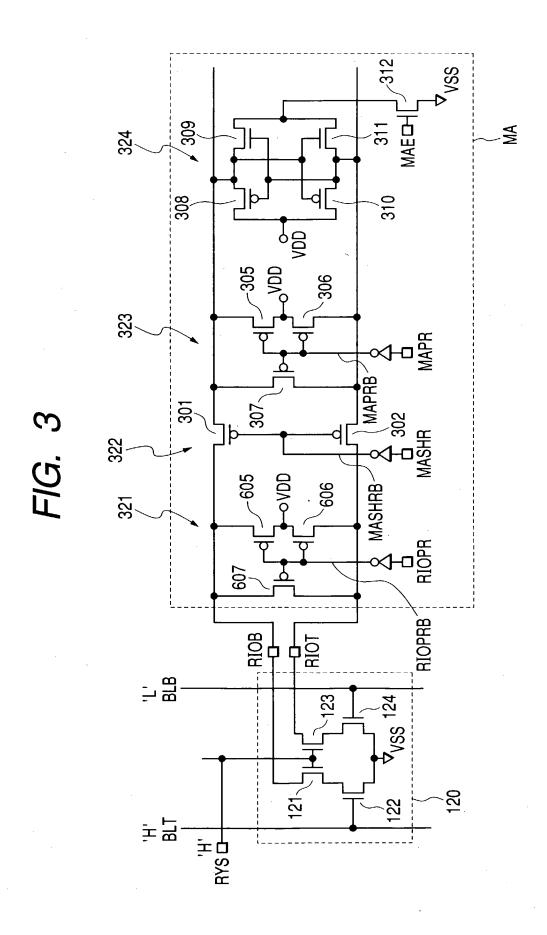
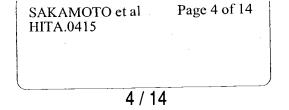


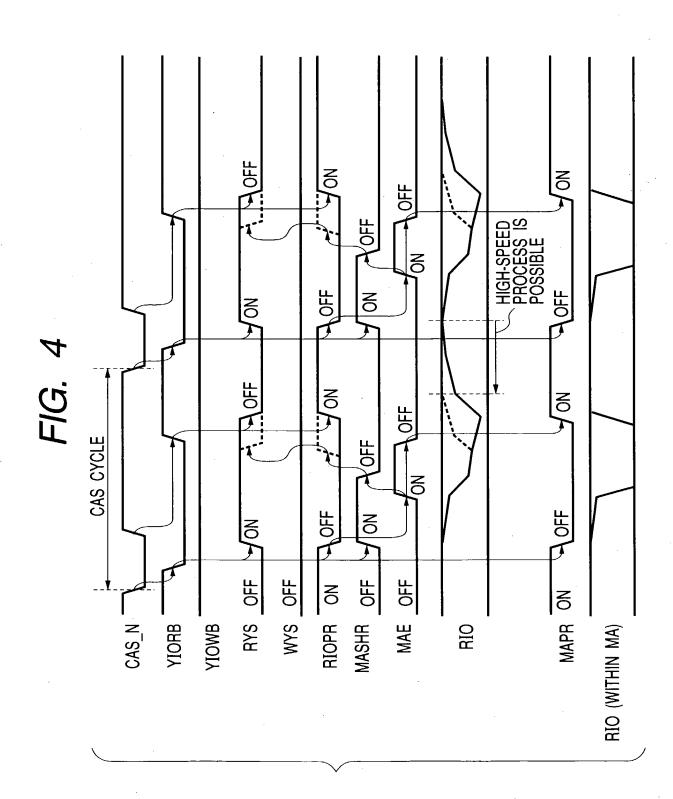
FIG. 2

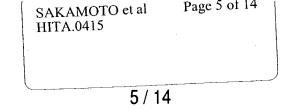


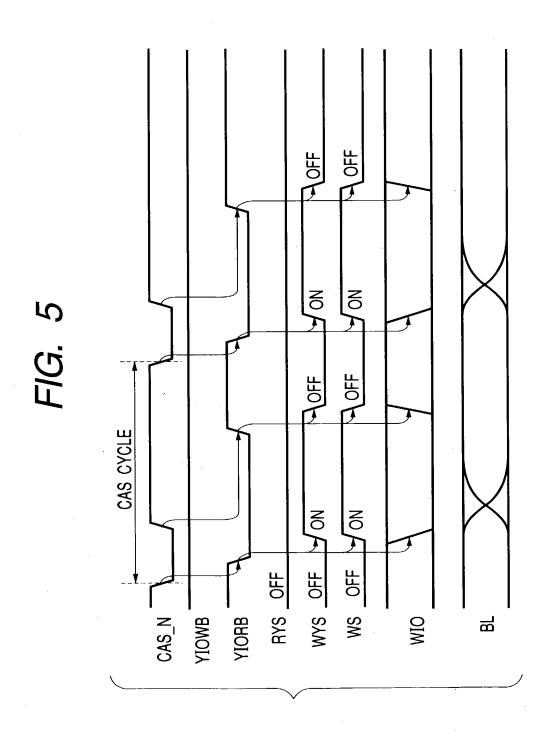












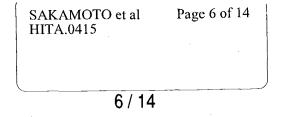


FIG. 6

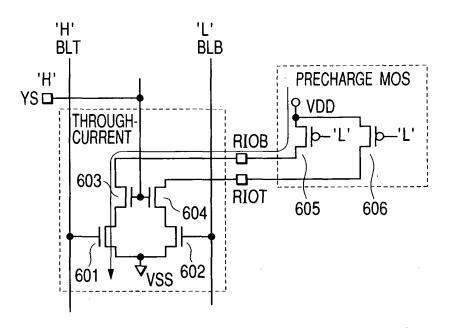
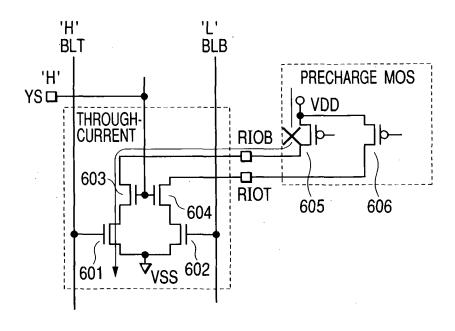
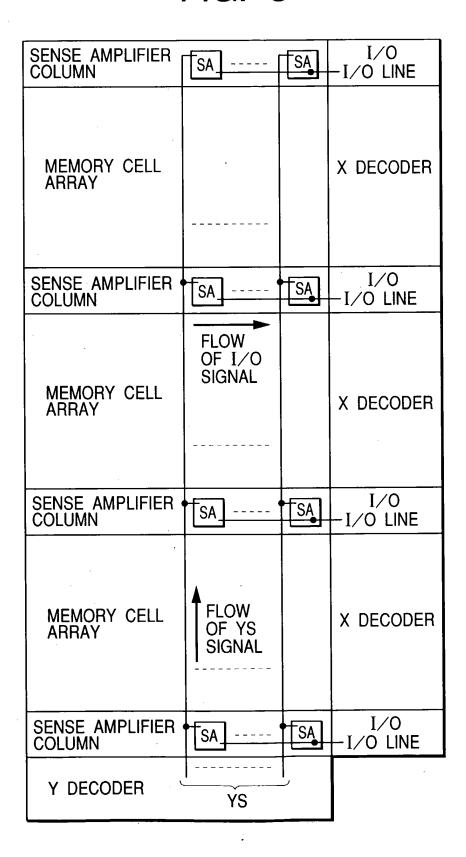


FIG. 7



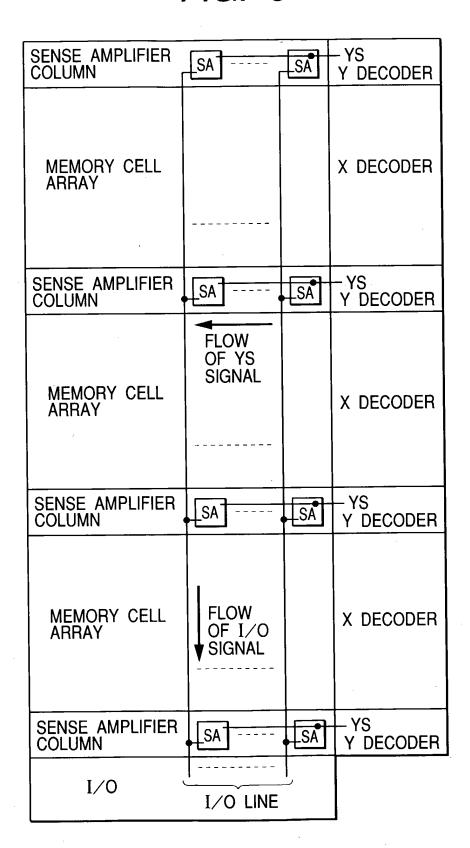
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FIG. 8

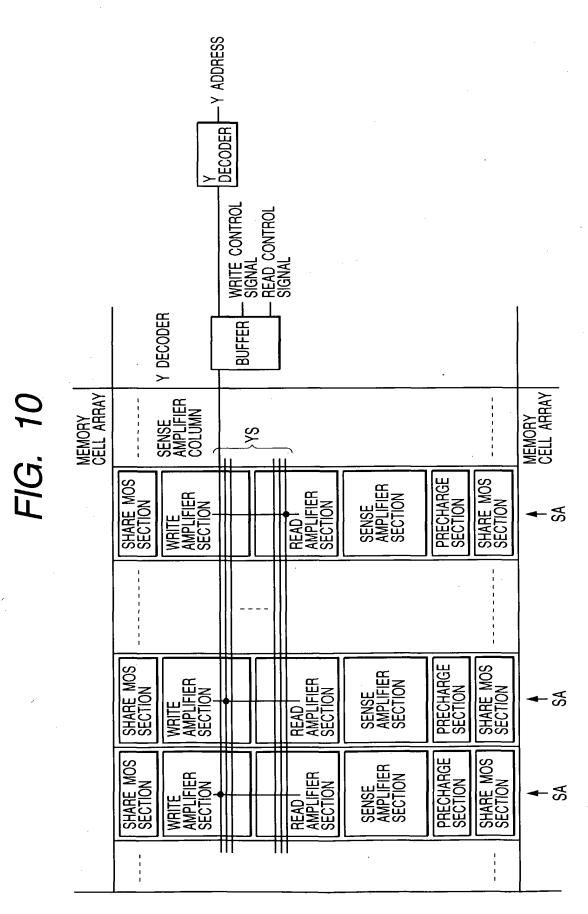


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FIG. 9



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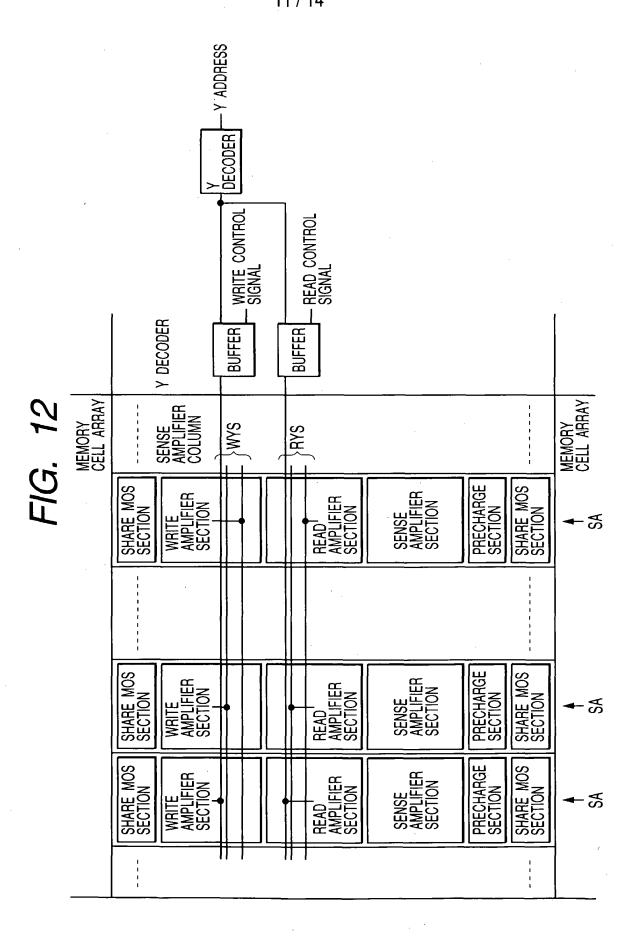


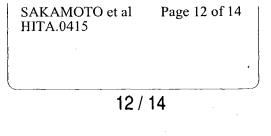
SENSE AMPLIFIER SECTION

SA

MEMORY CELL ARRAY

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DECODER - WRITE CONTROL SIGNAL - READ CONTROL SIGNAL Y DECODER BUFFER BUFFER FIG. 13 MEMORY CELL ARRAY MEMORY CELL ARRAY SWX> \RYS SHARE MOS SECTION SHARE MOS SECTION WRITE AMPLIFIER SECTION -S SHARE MOS SECTION WRITE AMPLIFIER SECTION PRECHARGE SECTION SHARE MOS SECTION SHARE MOS SECTION SENSE AMPLIFIER SECTION WRITE AMPLIFIER SECTION READ AMPLIFIER SECTION SA-

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FIG. 14

